A proof of concept balanced mixer with the use of a digital IF power combiner to improve LO noise rejection

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JAIN 2023 3.Analog design 1.Balanced Mixer Architecture 5.Results

 $I_{mixer} = 1/2(V_{RF} + (V_{LO} + noise_{LO}))^2 + \dots$

• The quadratic term of expansion causes that the noise near the pure sinusoidal LO, got also downconverted to the IF.





• This is a problem for system that uses several frequency multiplication chains to obtain a high LO frequency, since each stage adds noise to the LO.



Fig. 1: Traditional balanced mixer diagram.

- The usage of an hybrid and two opposite orientated diodes in the balanced mixer architecture causes the cancellation of the downconverted LO noise.
- The non-ideal behaviour of the built components limitates the LO noise cancellation.

(a) Photograph of the constructed mixer

b) Measured Conversion losses.

Fig. 3: Constructed mixer in the Ku-band.

- Since there is not commercial balanced mixer without the combiner stage, we built a mixer working in the Ku-band (13-15GHz).
- As the laboratory generators work injecting the minimum amount of noise, we built an artificial noise source to create a noisy LO.
- Since the artificial LO noise should present only in the bandwidth that its going to be downconverted we built a set of exchangeable filters.



(a) IF power of both ADCs when doing calibration (top), and total power received when utilizing an analog com- (b) Complex calibration constants (solid blue) and ideal values (dashed red) used for an LO frequency of 14 GHz

Fig. 5: Calibration measurements

- As the Figure 5 a) shows the amount of noise entering to the ADCs when no analog combiner is present is higher than when it is present, since when using the analog combiner the noise is rejected before the ADC.
- To compute the correction factors we used the noisy LO as the test signal to characterize the system. This is done to take in account the presence of USB and LSB in the IF.
- The Figure 5 b) shows the complex constants calculated over the bandwidth with the LO working at 14GHz.

2. Digitally calibrated balanced mixer



Fig. 2: Digitally calibrated balanced mixer diagram.

- The proposed system consists of replacing the analog combiner with an FPGA that corrects the imbalances and combines digitally the signals.



- Fig. 4: Test setup.
- As LO signal we utilized a generator combined with the artificial noise source.



(a) Noise temperature of the receiver over the entire IF (b) Noise temperature of the receiver over the entire RF spectrum, using a fixed LO of 14 GHz spectrum, averaged over 200 MHz of IF bandwidth

Fig. 6: Noise temperature measurements

- The Figure 6 a) shows the noise temperature for an LO working at 14GHz, obtaining lower temperatures than the analog combiner architecture.
- The Figure 6 b) shows the average noise temperature for different LO frequency values.
- For all LO frequencies the digitally cali-

- The FPGA model is composed by two subsistems.
 - 1. Calibration subsystem: An FX correlator that measure the imabalances of the system.
 - 2. Synthesis subsystem: With the imbalances measured we add the correction factors previous the combination of the signals coming from the hybrid.
- Since the balanced mixer is a dual-sided band receiver, we have mapped the USB and LSB to the same IF. This is a fundamental limitation on the correction factors computation.
- As RF source we utilize a noise diode to make a hot-cold test and determine the receiver temperature.
- To compare the performance of the proposed architecture and the standard balanced mixer, the final combiner is implemented analogically and digitally. We also measured the case of an analog combiner without added LO noise as a reference of the receiver performance.

brated combiner obtain lower noise temperatures than the analog combiner, and for certain points obtain comparable temperatures of the system without noise added to the LO.

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